

National Institute of Electronics & Information Technology Gorakhpur – Extension Centre Lucknow

(Ministry of Electronics and Information Technology, Government of India) MMMUT Campus, Deoria Road, Gorakhpur-273010 https://www.nielit.gov.in/gorakhpur/index.php



Course Content

VLSI Design using CADENCE Tool Duration: 20 Days (40 Hours)	
Module-1 (4 Weeks)	
Day-01	 Introduction to VLSI Design Historical Perspective. VLSI technology trends performance measures and Moore's law comparisons of technology trends. System approach to VLSI Design. Future Trends in CMOS VLSI Circuits and system design.
Day-02	 VLSI Design Cycle ASIC Design Flow. System Specification, Fundamental Design, Logic Design. Circuit Design, Physical Design, Design Verification. Fabrication, Packaging, Testing and Debugging. Introduction to Cadence tool.
Day-03	 Basics of Analog Circuits-1 Design and Analysis of RC circuits. Timing issues in RC Circuits. Filter Implementation of RC Circuits.
Day-04	Basics of Analog Circuits-2 • Operation Amplifiers Fundamentals. • Design and Analysis of feedback amplifiers. • Filter Implementation of Op-Amps.
Day-05	 Fabrication Process and Layout Design Rules-1 Introduction to fabrication Process. General Aspects of CMOS Technology.
Day-06	 Fabrication Process and Layout Design Rules-2 CMOS Inverter Fabrication Process. Layout Design Rules.
Day-07	 Analog CMOS Design-1 Basic of MOS Device Physics. General Concepts on Level of Abstraction. General Concepts on Robust Analog Design.



National Institute of Electronics & Information Technology Gorakhpur – Extension Centre Lucknow

(Ministry of Electronics and Information Technology, Government of India) MMMUT Campus, Deoria Road, Gorakhpur-273010 https://www.nielit.gov.in/gorakhpur/index.php



Day-08	 Analog CMOS Design-2 Way of designing fast CMOS Circuits. Design of Single Stage Amplifier. Analog Layout and Design Concepts.
Day-09 & Day-10	 Analog CMOS Design-3 Performance Analysis of an Amplifier. Transfer characteristics and Amplifier Gain. Effect of Amplifier BW limitations on Analog Signal Processing.
Day-11 & Day-12	 Digital CMOS Design-1 CMOS Inverter Basics. Inverter Transfer Characteristics. Inverter sizing.
Day-13 & Day-14	 Digital CMOS Design-2 Inverter Design. Transfer Function & Frequency Response. Characterization for various inputs and timing analysis.
Day-15 & Day-16 Day-17 to Day-19	 Combination Circuit Design-1 Digital CMOS implementation of Full Adder Circuit Output Verification. Timing and Power Analysis. Combination Circuit Design-2 Digital CMOS implementation of 4-bit Multiplier Circuit. Output Verification. Timing and Power Analysis.
Day-20	 Concluding Session Presentation & Reports. Feedback & Quiz.

Course Coordinator

Sh. Deepam Dubey (Scientist-C) NIELIT Gorakhpur, Email: deepamdubey@nielit.gov.in Mobile Number: +91-8317093874